VTRC
Virginia Transportation Research Council

We Bring Innovation to Transportation

Evaluation of Virginia Department of Transportation Chip Seal Practices: Materials and Design

https://vtrc.virginia.gov/media/vtrc/vtrc-pdf/vtrc-pdf/24-R6.pdf

ILKER BOZ, Ph.D.
Research Scientist

Final Report VTRC 24-R6

VIRGINIA TRANSPORTATION RESEARCH COUNCIL
530 Edgemont Road, Charlottesville, VA 22903-2454
vtrc.virginiadot.org

Standard Title Page - Report on Federally Funded Project

1. Report No.: FHWA/VTRC 24-R6	2. Government Accession No.:	3. Recipient's Catalog No.:
4. Title and Subtitle: Evaluation of Virginia Department of Transportation Chip Seal Practices: Materials and Design		5. Report Date: January 2024 6. Performing Organization Code:
7. Author(s): Ilker Boz, Ph.D.		8. Performing Organization Report No.: VTRC 24-R6
9. Performing Organization and Address: Virginia Transportation Research Council 530 Edgemont Road Charlottesville, VA 22903		10. Work Unit No. (TRAIS): 11. Contract or Grant No.: 118820
12. Sponsoring Agencies' Name and Address: Virginia Department of Transportation 1401 E. Broad Street Richmond, VA 23219 Federal Highway Administration 400 North 8th Street, Room 750 Richmond, VA 23219-4825		13. Type of Report and Period Covered: Final 14. Sponsoring Agency Code:
15. Supplementary Notes: This is an SPR-B report.		

16. Abstract:

It is crucial for highway agencies, including the Virginia Department of Transportation (VDOT), to maintain the structural and functional conditions of existing pavements in a state of good repair. Pavement preservation treatments can help achieve this objective by extending the service life of existing (flexible) pavements through delaying deterioration and improving the functional performance characteristics of these pavements. Chip seals are among the most commonly used pavement preservation treatments, and their performance highly depends on the characteristics of the materials used and their application (design) rates. In recent years, extensive research has been undertaken at the local and national levels to evaluate the effects of material characteristics and design techniques on the performance of chip seals. Further, new materials and additives have been introduced into the construction market with the aim of enhancing the performance of chip seals. Despite these advances and the long history of chip seal use on its roadway network, VDOT has not conducted a thorough review of its chip seal practices in more than 25 years.

This study assessed VDOT's single-layer chip seal practices, both conventional and modified, from the perspectives of materials characterization and design. In this effort, aggregates and emulsions from eight chip seal projects across Virginia were acquired for laboratory characterization. The materials were benchmarked using state-of-the-art methods and practices to determine how and if the current VDOT practice aligns with the nationally standardized practices. In addition, the field performance of these projects was monitored for up to 1.2 years using macrotexture as a performance metric. This was done to assess how the current design practice affects performance in the field.

The study concluded that based on rheological characteristics, the emulsion used in chip seals may not be suitable for the conditions (traffic and climate) in which they were used. Conversely, the physical characteristics of the chip seal aggregates were suitable for the conditions (traffic) in which the chip seals were used. In addition, VDOT's chip seal design practices for the single-layer chip seals may not be suitable. Further, the study concluded that more vigorous quality measurement practices are essential for improved or optimal performance of chip seals.

The study recommends that (1) AASHTO MP 37, used for performance grading of emulsions (residues), be adopted for optimized chip seal performance; (2) the traffic-based requirements for abrasion loss and flakiness index as specified in AASHTO M 340 be adopted to specify performance requirements for chip seal aggregates; (3) AASHTO R 102 be adopted as the standard used for chip seal design; and (4) more vigorous quality control measurement practices be explored by VDOT to further improve the performance of chip seals in the field. It is anticipated that implementing these recommendations will help achieve the desired outcome of chip seals: longer service life, larger cost savings, reduced user delays, and safer roads.

17 Key Words: Chip seals, surface treatment, materials, aggregates, emulsions, performance grading, chip seal design, performance, macrotexture, mean profile depth.	18. Distribution Statement: No restrictions. This document is available to the public through NTIS, Springfield, VA 22161.

19. Security Classif. (of this report): Unclassified	20. Security Classif. (of this page): Unclassified	21. No. of Pages: 32	22. Price:

Form DOT F 1700.7 (8-72) Reproduction of completed page authorized

FINAL REPORT

EVALUATION OF VIRGINIA DEPARTMENT OF TRANSPORTATION CHIP SEAL PRACTICES: MATERIALS AND DESIGN

Ilker Boz, Ph.D.
Research Scientist

In Cooperation with the U.S. Department of Transportation
Federal Highway Administration

Virginia Transportation Research Council
(A partnership of the Virginia Department of Transportation
and the University of Virginia since 1948)

Charlottesville, Virginia

January 2024
VTRC 24-R6

DISCLAIMER

The contents of this report reflect the views of the author, who is responsible for the facts and the accuracy of the data presented herein. The contents do not necessarily reflect the official views or policies of the Virginia Department of Transportation, the Commonwealth Transportation Board, or the Federal Highway Administration. This report does not constitute a standard, specification, or regulation. Any inclusion of manufacturer names, trade names, or trademarks is for identification purposes only and is not to be considered an endorsement.

ABSTRACT

It is crucial for highway agencies, including the Virginia Department of Transportation (VDOT), to maintain the structural and functional conditions of existing pavements in a state of good repair. Pavement preservation treatments can help achieve this objective by extending the service life of existing (flexible) pavements through delaying deterioration and improving the functional performance characteristics of these pavements. Chip seals are among the most commonly used pavement preservation treatments, and their performance highly depends on the characteristics of the materials used and their application (design) rates. In recent years, extensive research has been undertaken at the local and national levels to evaluate the effects of material characteristics and design techniques on the performance of chip seals. Further, new materials and additives have been introduced into the construction market with the aim of enhancing the performance of chip seals. Despite these advances and the long history of chip seal use on its roadway network, VDOT has not conducted a thorough review of its chip seal practices in more than 25 years.

This study assessed VDOT's single-layer chip seal practices, both conventional and modified, from the perspectives of materials characterization and design. In this effort, aggregates and emulsions from eight chip seal projects across Virginia were acquired for laboratory characterization. The materials were benchmarked using state-of-the-art methods and practices to determine how and if the current VDOT practice aligns with the nationally standardized practices. In addition, the field performance of these projects was monitored for up to 1.2 years using macrotexture as a performance metric. This was done to assess how the current design practice affects performance in the field.

The study concluded that based on rheological characteristics, the emulsion used in chip seals may not be suitable for the conditions (traffic and climate) in which they were used. Conversely, the physical characteristics of the chip seal aggregates were suitable for the conditions (traffic) in which the chip seals were used. In addition, VDOT's chip seal design practices for the single-layer chip seals may not be suitable. Further, the study concluded that more vigorous quality measurement practices are essential for improved or optimal performance of chip seals.

The study recommends that (1) AASHTO MP 37, used for performance grading of emulsions (residues), be adopted for optimized chip seal performance; (2) the traffic-based requirements for abrasion loss and flakiness index as specified in AASHTO M 340 be adopted to specify performance requirements for chip seal aggregates; (3) AASHTO R 102 be adopted as the standard used for chip seal design; and (4) more vigorous quality control measurement practices be explored by VDOT to further improve the performance of chip seals in the field. It is anticipated that implementing these recommendations will help achieve the desired outcome of chip seals: longer service life, larger cost savings, reduced user delays, and safer roads.

FINAL REPORT

EVALUATION OF VIRGINIA DEPARTMENT OF TRANSPORTATION CHIP SEAL PRACTICES: MATERIALS AND DESIGN

Ilker Boz, Ph.D.
Research Scientist

INTRODUCTION

Overview

Sustaining and improving the structural and functional conditions of existing pavements in a state of good repair are among the important operational actions of any highway agency. Pavement preservation treatments contribute to this objective by enhancing the functional performance characteristics (e.g., restoring surface integrity and texture) of existing pavements. In addition, these treatments extend the service life of pavements by delaying deterioration through minimizing moisture infiltration and slowing down aging of flexible pavements (Boz et al., 2018). All of these benefits, in turn, result in reduced life-cycle costs, which are of particular interest to highway agencies facing budget limitations while striving to maintain the roadway network in a good condition.

Among the various types of surface treatments, chip seals comprise the most commonly used treatment method in the United States (Gransberg and James, 2005). In addition to the aforementioned benefits, the ease and cost of construction compared to other alternatives make chip seals an appealing treatment method for pavement preservation (Boz et al., 2019). Despite their widespread use, the service life (performance) of chip seals across the United States has shown significant variation, with a typical range of 3 to 20 years (Pierce and Kebede, 2015). Although the performance of chip seals depends on many condition-based factors (e.g., existing pavement, traffic, and climate) and non–condition-based factors (e.g., material properties and their application rates and construction practices), one of the main reasons for such a high variation in performance can be attributed to the lack of using proper constituent materials (aggregates and emulsions or binders) and the lack of employing engineered design procedures for these treatments (Gransberg and James, 2005).

Material characteristics have a direct impact on the performance of chip seals. Improper selection of materials leads to premature failures or a shorter lifespan than could have been achieved with properly designed and applied treatments. For instance, the literature documents aggregate loss and bleeding as the most commonly observed modes of distress, mainly due to the improper use of material properties and excessive or insufficient material application rates (Boz et al., 2018; Gransberg and James, 2005; Kumbargeri et al., 2018a, 2019, 2021; Pierce and Kebede, 2015).

The application (design) rates of the constituent materials of chip seals are mostly determined based on empirically developed and outdated methods (in some cases, dating back

several decades) or based on standard application rates established due to historical experience with the performance of chip seal materials but having no basis in engineering design (Gransberg and James, 2005). The applicability of empirical-based approaches is valid only for the materials, traffic, and climatic regions for which the methods were developed. As characteristics of materials used in treatments, traffic volumes, and aging of subsurface pavement conditions change, these approaches may become obsolete with today's construction practices. Using standard application rates that are not based on an engineered approach provides only a single "solution" for each pavement candidate, disregarding the factors affecting the performance of chip seals.

Given these limitations in chip seal practices, extensive research has been conducted in recent years at the local and national levels to investigate the effects of material characteristics and design techniques on the performance of chip seals. In addition, with the advancement of technology, new materials and additives have been introduced into the construction market with the goal of enhancing the performance of chip seals. Despite these advances, and the long history of chip seal use on its roadway network, the Virginia Department of Transportation (VDOT) has not undertaken a thorough review of its chip seal practices in more than 25 years (Maupin and Payne, 1995).

Background

Basic Concepts

Chip seals have been used as a method for re-surfacing pavements since the 1920s (Boz et al., 2018). New low-volume roads were initially constructed using chip seals. Over the last two decades, the use of chip seals has transformed into a maintenance and preservation treatment for lightly deteriorated pavements (Boz et al., 2018). As a preservation treatment, a chip seal consists of an application of a layer(s) of emulsified asphalt binder (or hot asphalt binder) on an existing pavement followed by the spreading of an aggregate layer(s) over the surface and compaction with rollers, typically pneumatic rollers (Boz et al., 2018). The binder layer in chip seals acts as a waterproof layer to prevent moisture infiltration and reduce aging of the underlying pavement, whereas the aggregate layer improves skid resistance and furnishes protection to the asphaltic layer from tire damage (Janisch and Gaillard, 1998).

Various types of chip seal applications are used in practice. Gransberg and James (2005) provide details on different types of chip seals. Among these, single-layer chip seals are the most common, followed by multilayer chip seals. Single-layer chip seals are defined as one application of the bituminous binder (emulsion or hot binder) followed by one application of uniformly graded cover aggregate. Multilayer chip seals are defined as the multicourse alternating applications of bituminous binders and aggregates. In VDOT's special provision for chip seals, also referred to as asphalt surface treatments (SP314-000100-00), three types of chip seal applications are defined: single treatment (single-layer chip seals), modified single seals, and modified double seals.

- A modified single seal is defined as two applications of asphalt material, one application of cover aggregate and one application of blot fine aggregate.

- A modified double seal is defined as three applications of asphalt material, two applications of cover aggregate and one application of blot fine aggregate.

The modified single and multicourse chip seal applications were introduced to VDOT to overcome the problems encountered with conventional (i.e., unmodified) chip seals (Maupin and Payne, 1995). The modified single-layer chip seal application is the most common chip sealing technique used in Virginia.

The desired performance of chip seals is achieved by closely following the best practices in designing and constructing such treatments. As indicated previously, several factors affect the performance of these treatments, such as design practices, condition of the existing pavement, quality of the materials being used, construction practices, climate, and traffic. The performance of such treatments as it relates to the design is affected by the interaction of aggregate and emulsion/binder. This interaction is dominated by the application rates of aggregate and binder and their properties, such as aggregate size and shape, gradation, and stiffness (Boz et al., 2019). When these factors are not properly taken into consideration, premature failure of chip seals is inevitable. As indicated earlier, the two major distresses related to chip seals are aggregate loss (or raveling) and bleeding. The frequent occurrence of these distresses is generally related to poor-quality materials (e.g., soft emulsions/binders, dusty aggregates, incompatible materials) and/or insufficient or excessive application rates (Gransberg and James, 2005). For example, low emulsion application rates and/or high aggregate application rates are the main driving factors of aggregate loss. On the other hand, bleeding, for example, results from high emulsion application rates and/or low aggregate application rates. These examples highlight the importance of properly selecting chip seal constituent materials and using a rational chip seal design process to achieve satisfactory performance of chip seals.

Emulsions

Although asphalt cements and cutback asphalts can also be used, the most commonly used binding agent in chip seals is an asphalt emulsion (Pierce and Kebede, 2015). Emulsions are the only specified asphalt materials for use in VDOT's chip seal specification and were thus the focus of this study.

Emulsions are derived by milling asphalt into microscopic particles and dispersing them in water with chemical emulsifier. Emulsions can also include other additives such as polymers for enhanced performance. The classification of asphalt emulsions is based on the electrical charges on the surface of droplets in the asphalt binder. Cationic emulsions have positive charges and are denoted with a C, whereas anionic emulsions have negatively charged droplets and do not have a prefix of C. Further classification is made based on setting or breaking times: rapid setting, medium setting, and slow setting (Cross and Jakatimath, 2007). Cationic rapid setting (CRS) emulsions (unmodified) are the most commonly used emulsion types in the United States, and the use of modified (polymer or latex) CRS emulsions in chip seals has steadily increased due to improved performance (Kim et al., 2017). The VDOT specification allows for the use of both unmodified and modified rapid setting emulsions in chip seal applications.

As indicated, the function of emulsions in chip seals is to act as a waterproof layer to prevent moisture infiltration and reduce aging of the underlying pavement, bond to the aggregates, and adhere to the existing pavement surface. The physical, chemical, and rheological characteristics of emulsions play a key role in performance. The physical and chemical characteristics of emulsions to be used in chip seal applications are standardized by AASHTO and are referred to in VDOT's chip seal specification. Specifically, the specification requires that emulsions be tested in accordance with the following AASHTO standards: AASHTO M 208, AASHTO M 316, AASHTO T 59, and AASHTO T 301. Where applicable, the specification provides certain exceptions to the standards. For example, VDOT differs from AASHTO M 316 in that it requires a minimum elastic recovery for CRS-2L emulsion of 50%.

Ample literature indicates the importance of the rheological properties of emulsified asphalt residue in controlling chip seal distresses, particularly bleeding and aggregate loss (Islam and Hossain, 2011; Johannes et al., 2011; Miller et al., 2010; Shuler et al., 2011; Wasiuddin et al., 2013). This was further explored in NCHRP Project 09-50 to establish performance-based specifications for emulsions used in chip seals and other types of surface treatments (microsurfacing and spray seals). The project resulted in a report by Kim et al. (2017) with a set of performance-related (mainly rheology-based) specifications for emulsified asphaltic binders used in preservation surface treatments, including chip seals. The recommended specifications are climate driven and applicable to the traffic loads to which the preservation treatments are subjected during their service life. Kim et al. (2017) included draft specifications for performance-graded emulsions used in chip seals. The proposed specifications cover some of the existing AASHTO standards, such as AASHTO T 44, AASHTO T 59, AASHTO T 50, and AASHTO R 78, which are mainly related to physical and chemical characteristics of emulsions, and are directly or indirectly referenced in VDOT's specification for chip seals. The proposed specifications also introduced modifications to existing AASHTO standards, along with performance criteria for pavement preservation treatments, including chip seals. Moreover, Kim et al. (2017) proposed modifications to AASHTO T 316 (Standard Method of Test for Viscosity Determination of Asphalt Binder Using Rotational Viscometer) to evaluate sprayability and drain-out resistance characteristics of emulsions used in chip seals and established performance criteria for emulsions to be used in those treatments. These performance-related specifications, which are not part of VDOT's chip seal specification, are briefly discussed later.

In 2016, AASHTO published a provisional standard for materials used in emulsified asphalt chip seals (AASHTO MP 27), which was adopted as a full standard in 2022, designated AASHTO M 340. The standard references the existing AASHTO standards (AASHTO M 140, AASHTO M 208, and AASHTO M 316) for emulsion properties, mainly related to physical and chemical properties of emulsions. These standards are also referred to in the VDOT specifications. In 2018, AASHTO published a provisional specification for performance-graded asphalt binder for surface treatments, including emulsions used in chip seals (AASHTO MP 37). This provisional specification covers asphalt binders (emulsions) for seal coat and chip seal applications graded by performance. Performance grading designations are related to the average 7-day maximum pavement *surface* design temperature and the minimum pavement *surface* design temperature. This provisional standard follows a similar testing campaign conducted for performance-graded asphalt binders used in hot mix applications in accordance with AASHTO M 320.

Aggregates

Aggregate characteristics that play a key role in achieving satisfactory chip seal performance include particle size distribution (gradation), specific gravity, unit weight, aggregate absorption, and flakiness ratio. These properties are used as input parameters in various chip seal design procedures to estimate aggregate application rates. They are also used for quality measurement practices and comparative performance ranking of chip seals (Boz et al., 2018).

Aggregate gradation and size are among the main factors affecting chip seal performance (Johannes et al., 2011; Lee and Kim, 2009; Wasiuddin et al., 2013). Chip seals with uniformly graded aggregates are more resistant to distresses compared to chip seals with well-graded aggregates provided all other characteristics are maintained the same. The aggregate gradation uniformity can be quantified through the use of various parameters such as the uniformity coefficient and performance-based uniformity coefficient (Das and Sobham, 2013; Lee and Kim, 2009). Aggregate size is an important parameter to consider in chip seals, as the aggregate must offset the gradual embedment into the pavement substrate due to traffic loading while still being able to maintain adequate pavement macro- and microtexture characteristics (Buss et al., 2016). The nominal aggregate size of 9.5 mm (3/8 in) is the most commonly used size in chip seal applications in the United States (Pierce and Kebede, 2015). AASHTO M 340 lists four aggregate gradation types for chip seals, whereas VDOT's chip seal specification requires a single gradation (No. 8P) with a nominal aggregate size of 9.5 mm.

The majority of state highway agencies in the United States limit the use of flaky aggregates in chip seals due to their negative impact on chip seal performance (Boz et al., 2018). Flat particles are more prone to orient with the longest axis embedded in the roadway, thereby reducing surface texture, which hinders one of the main purposes of chip seal applications (Buss et al., 2016). In addition, chip seals with flaky aggregates create an unstable chip seal structure, resulting in aggregate loss and bleeding problems, as well as a potential degradation/crushing of aggregates under traffic loading (Kumbergari et al., 2020). Many agencies use ASTM D4791 to determine the percent flat and elongated particles using material sieved during the standard mechanical analysis test. This test method also covers the determination of the percentage of flaky particles in coarse aggregates. The main intent for this standard was as a specification for aggregates used in hot mix asphalt production, but it has also been used by some agencies (e.g., VDOT) as a specification for use in chip seal applications. VDOT requires a maximum 20% flakiness ratio, irrespective of traffic volume, as measured in accordance with ASTM D4791. Several agencies, such as the Minnesota Department of Transportation (DOT) and the Texas DOT, use the slotted metal plate (flakiness gauge) to determine the percent flaky aggregates. This flakiness index (ratio) test is performed in accordance with the procedure implemented by the Minnesota DOT for seal coat aggregates to determine the percentage of flat particles in each aggregate source. AASHTO M 340 recommends this test to determine the flakiness ratio of chip seal aggregates and limits the flakiness ratio with respect to three different traffic levels.

The angularity of the aggregate indicates the tendency of chip seals to be damaged by stopping or turning traffic. Rounded aggregates are prone to displacement by traffic because they provide the least interfacial area between the aggregate and binder. The roundness of the aggregate determines how resistant chip seals will be to turning and stopping movements

(Gransberg and James, 2005). AASHTO M 340 requires that a certain percentage of the aggregate, as measured in accordance with AASHTO T 335, have at least two fractured faces based on the traffic volume. VDOT's specification requires that crushed gravel consist of aggregate particles of at least 80% by weight with at least one face fractured, as determined in accordance with Virginia Test Method 15. This requirement does not account for traffic volume. In addition, chip seal aggregate shape and texture characteristics (i.e., angularity and sphericity) impact the quality of the bond formed between the aggregate and emulsion/binder (Buss et al., 2016). Although no national standards are available to practically quantify and standardize these aggregate properties, several studies have used digital image processing and analysis techniques for that purpose. One example of such a study undertaken for the Oklahoma DOT quantified texture characteristics for chip seal aggregates (Zaman et al., 2013). It should be noted that there are currently two newly adopted AASHTO standards available to determine aggregate shape characteristics by means of digital image analysis: AASHTO R 91, Standard Test Method for Determining Aggregate Source Shape Values From Digital Image Analysis Shape Properties, and AASHTO T 381, Standard Test Method for Determining Aggregate Shape Properties by Means of Digital Image Analysis.

Aggregates used in chip seals should also be resistant to abrasion. Common tests for measuring abrasion resistance are the Los Angles abrasion test (AASHTO T 96), which is specified by VDOT, and the Micro-Deval test (AASHTO T 327). These tests represent the degradation during transport, mixing, and compaction and the ability to withstand heavy wheel loading (Buss et al., 2016). VDOT specifies a single abrasion value depending on the aggregate type used, whereas AASHTO M 340 specifies traffic-based abrasion values as determined in accordance with AASHTO T 96. In addition to the aggregate characteristics discussed in the preceding paragraphs, chip seal aggregate must be free from deleterious materials, clean (with no excessive fine materials or dust) to the extent possible, and compatible with the asphalt emulsion. It should be noted that the VDOT specification requires that the compatibility test be conducted in accordance with Virginia Test Method 65 and requires aggregates to be washed to eliminate the detrimental effect of dust (weakening the adhesive bond between aggregate and emulsion) and increase the adhesion between the constituent materials.

Chip Seal Design

Implementation of a proper design that accounts for the previously mentioned condition-based and non–condition-based factors together with sound construction practices will lead to achieving the desired performance for chip seals: longer service life, greater cost savings, and reduced user delays (Buss et al., 2016). Chip seal design methods mainly consist of two fundamental categories: empirical design based on experience, and engineered design based on some form of engineering algorithm (Gransberg and James, 2005). With experience-based design, the design starts with a base rate for both emulsion and aggregate and evolves from years of experience in the field. Engineering-based design involves determining the grade, type, and application rate for an emulsion, given the aggregate size and type, surface condition of existing pavement, traffic volume, and actual type of chip seal being used. Several countries, such as Australia, New Zealand, and South Africa, have developed engineering-based chip seal design methods (Gransberg and James, 2005).

In the United States, chip seal design has been reported to be somewhat of an art rather than a science (Gransberg and James, 2005). The majority of highway agencies rely on locally developed empirical procedures. Nevertheless, there have been efforts to develop design procedures by numerous researchers. The modified Kearby method and the McLeod method are popular design procedures that have been adopted by some agencies in combination with empirical experience (McLeod, 1969; Texas DOT, 2010). The McLeod design method was adopted as a design process by the Asphalt Institute, and it is the method specified in VDOT's chip seal specification for single-layer chip seals. It should be noted that the McLeod method was modified by researchers (Johannes et al., 2011) to eliminate some of the basic assumptions relating to the volume of void content in the compacted structure of chip seals.

In the McLeod design method, the required quantities of emulsion and aggregate are determined using mathematical equations. The aggregate application rate involves determining gradation, the average least dimension of aggregates, the voids in the cover aggregate, and the bulk specific gravity. The binder application rate is determined as a function of the aggregate gradation, pavement condition, and traffic volume. The correction factors for the quantity of binder lost due to the absorption of aggregate and the texture of the existing surface are also recommended. The McLeod design method assumes that the volume of air voids in aggregates is 50% of the total volume at the time of chip seal aggregate spreading and reduces to 30% after compaction and 20% after sufficient traffic (Johannes et al., 2011). The asphalt binder or emulsion is expected to fill 65% to 70% of the final air voids. The modified McLeod method recommends that the final void content be 40%, instead of the 20% assumed in the original McLeod method. The equations for binder and aggregate application rates are modified accordingly (Johannes et al., 2011). Both methods assume aggregates orient on their flattest side in the field.

As indicated, the McLeod design method was adopted as a chip seal design method by the Asphalt Institute. VDOT's chip seal specification refers to the *Asphalt Institute Manual* for determining emulsion and aggregate application rates for single-layer chip seals, rather than referring to the original source. The *Asphalt Institute Manual* does not provide the mathematical equations involved in the design method but rather provides tables that indicate a range of emulsion and aggregate application rates for a given aggregate. The application ranges provided in the tables are based on an aggregate specific gravity of 2.65 and are very wide. For example, for No. 8 aggregates, the application rates range from 20 to 25 lb/sy for aggregates and 0.20 to 0.35 gal/sy for emulsions. VDOT adopted this design method in 1985 (Maupin and Payne, 1995), and no changes to the specification from the design perspective have been made since then. It is also worth mentioning that VDOT specifies prescribed emulsion and aggregates rates for modified single-layer chip seals.

The modified Kearby method is used by the Texas DOT and many other road agencies. This method is now standardized by AASHTO; it was first published as a provisional standard in 2016, as AASHTO PP 82, and then as a full standard in 2022, as AASHTO R 102. The so-called "board test" is used to determine the aggregate quantity that fits one-layer-thick aggregates in 1 yd^2. In this test, aggregates are placed on a board measuring 3 by 1½ ft until every gap is filled and a one-stone-thick layer is formed. The quantity of the aggregates placed is multiplied by a factor of 2 and selected as the design application rate. The emulsion application rate is

determined as a function of the aggregate gradation, pavement condition, traffic volume, and percent embedment of aggregates. This method assumes that the aggregates orient on their flattest side in the field. The referenced standards relating to the materials characteristics in AASHTO R 102 are also referred to in VDOT specifications.

In recent years, performance-based design procedures have also been proposed by several researchers to determine optimal application rates for chip seals. These procedures involve laboratory tests to minimize chip seal primary distresses (aggregate loss and bleeding) and to determine optimal application rates (Adams and Kim, 2011; Kumbargeri et al., 2018b).

PURPOSE AND SCOPE

The purpose of this study was to evaluate VDOT's single-layer chip seal practices, both conventional and modified, from the standpoint of materials characterization and design. This evaluation was performed on the materials and designs that are typically used for chip seal applications in Virginia. The goal was to compare the current local practices to the nationally standardized practices. Thus, chip seal constituent materials obtained from eight field projects across Virginia were benchmarked using state-of-the art methods and practices. In addition, the performance of these chip seal projects was monitored to evaluate the performance of the current design practice in the field, using macrotexture as a performance parameter.

METHODS

Materials

The aggregates and emulsions used in this study were sampled from eight randomly selected chip seal projects across Virginia during the 2021 construction season. Table 1 presents the location and traffic details of these projects. All projects consisted of modified single-layer chip seals executed by contractors except for Project 3, which was a single-layer chip seal project applied by VDOT's residency forces. The aggregate samples were collected from the first layer and the second layer applications of the modified single-layer chip seal projects. The same emulsion type that was used for both emulsion applications was also sampled from each project. For Project 3, samples were collected from a single application of aggregate and emulsion.

Table 1. Selected Field Projects for Evaluation

Project ID	Route	County	District	Route Name	ADT
1	609	Mecklenburg	Richmond	Tinker Road	250-399
2	660	Brunswick	Richmond	Siouan Road	400-749
3	730	Southampton	Hampton Roads	Whitehead Road	100-249
4	1221	Northumberland	Fredericksburg	Riverview Road	25-49
5	633	Caroline	Fredericksburg	Nancy Wrights Drive	100-249
6	647	Appomattox	Lynchburg	Little Dogwood Road	50-99
7	628	Cumberland	Lynchburg	Forest View Road	100-249
8	633	Botetourt	Salem	Glen Wilton Rd	400-749

ADT = average daily traffic.

Test Methods

Emulsion Properties

Emulsion Viscosity

The viscosity of the emulsions was tested in accordance with AASHTO T 316 in conjunction with the procedure recommended by Kim et al. (2017) in NCHRP Project 09-50. The viscosity testing was conducted to evaluate the sprayability and drain-out resistance characteristics of the emulsions with respect to the performance criteria established as part of the NCHRP study. The sprayability refers to the ability of an emulsion to be sprayed uniformly over the existing pavement surface, and the drain-out resistance refers to the ability of an emulsion to resist draining off the pavement surface due to gravity (Kim et al., 2017; Rizzutto et al., 2015). Emulsions with poor sprayability and drain-out resistance characteristics can cause early chip seal failures such as streaking and aggregate loss (Johannes and Bahia, 2013). As part of the viscosity test, also known as the three-step shear test, a rotational viscometer is used to apply various levels of shear rates to an emulsion in three steps at a specified temperature. An emulsion is first tested at a shear rate of 4.65 s^{-1} (equivalent to 5 revolutions per minute [RPM]) for 15 minutes, which represents the pumping and handling conditions of the emulsion before spraying in the field. Then, the emulsion is tested at a shear rate of 142 s^{-1} (equivalent to 150 RPM) for 5 minutes. This step is assumed to mimic the spraying of the emulsion through a nozzle. Finally, the emulsion is again tested at a shear rate of 4.65 s^{-1} (equivalent to 5 RPM) for 5 minutes, which simulates the emulsion's resistance to flow off under gravitational forces after being sprayed in the field. No rest periods between the steps were introduced. Although no limits were specified for the first step, the NCHRP study set a maximum limit of 400 centipoise for the second step and a minimum limit of 50 centipoise for the third step. The emulsions used in this study were tested using a single replicate measurement at a temperature of 60°C.

Emulsion Residue Content

The residual asphalt contents of the emulsions were determined using four replicate measurements in accordance with AASHTO T 59, Section 7. The residual asphalt content is used as an input parameter in chip seal design procedures to estimate emulsion application rates, and it is also used for quality measurement practices. For example, VDOT requires a minimum of 65% emulsified asphalt residue for an emulsion to be eligible for use in chip seals.

Emulsion Residue Rheology

The emulsions (residues) were performance graded in accordance with AASHTO M 37. As indicated earlier, performance grading designations are determined based on the average 7-day maximum pavement surface design temperature and the minimum pavement surface design temperature. Surface-grade temperatures are generally 3°C greater (for high-temperature grade) or lower (for low-temperature grade) than those determined for hot mix asphalt performance-graded binders. Thus, the emulsions (residues) were evaluated at temperatures of 67°C and −25°C in this study. The recovery of the emulsion residues was performed in accordance with AASHTO R 78, Method B. The testing for determination of the high-temperature performance

grade (PG) was conducted in accordance with AASHTO T 315 on the as-recovered emulsion residues. On the other hand, the testing for determination of the low-temperature PG was conducted in accordance with AASHTO T 313 on the as-recovered emulsion residues after they were subjected to aging in the pressurized aging vessel in accordance with AASHTO R 28. The emulsion residues are not subjected to the rolling thin-film oven test conducted in accordance with AASHTO T 240. It should be noted that the performance criteria set forth in AASHTO M 37 for emulsion residues are different than those used for conventional binders as determined in accordance with AASHTO M 320.

Kim et al. (2017), in NCHRP Project 09-50, recommended the non-recoverable creep compliance (J_{nr}) parameter measured at a stress level of 3.2 kPa at a specified temperature to assess the contribution of an emulsion residue to the bleeding potential of chip seals. They defined three traffic classes based on the annual average daily traffic (AADT) for emulsions used in chip seal applications. These traffic classes are low-volume traffic for AADT less than 500; medium-volume traffic for AADT between 501 and 2,500; and high-volume traffic for AADT greater than 2,500 vehicles. In this study, the emulsion residues were tested at 67°C in accordance with AASHTO T 350. The J_{nr} performance limits established at 67°C for the low-, medium-, and high-volume traffic levels were 8, 5.5, and 3.5 kPa^{-1}, respectively.

Kim et al. (2017) also proposed the dynamic shear rheometer frequency sweep test to evaluate the low-temperature aggregate loss resistance of chip seals. For this evaluation, the dynamic shear modulus (|G*|) at a critical phase angle (δc) is used. The δc is specified as a function of the low-temperature surface PG of a climatic region of interest. For Virginia, the δc is 45°, considering the minimum pavement surface temperature of -25°C. As per Kim et al. (2017), the |G*| limits at the δc of 45°C for low-, medium-, and high-volume traffic levels are 30, 20, and 12 MPa, respectively. The dynamic frequency sweep tests, at temperatures of 5°C and 15°C with a frequency range from 1 to 100 rad/s, were performed in accordance with AASHTO T 315 on the as-recovered emulsion residues used in this study. The |G*| master curve for each emulsion reside was constructed using the Christensen-Anderson-Marasteanu model (Marasteanu and Anderson, 1999) at a reference temperature of 15°C. The optimized fitting parameters obtained from the |G*| master curve were used to construct the δ master curve for each emulsion. From the δ master curve, the reduced frequency that corresponded to the δc of 45° was identified. Then, the |G*| value at that reduced frequency was determined and used to assess the contribution of an emulsion residue to the aggregate loss potential of chip seals.

Aggregate Properties

The aggregate properties characterized in this study were particle size distribution (gradation), specific gravity, unit weight and voids in unit volume of aggregates, and the flakiness ratio. These physical properties are used as input parameters in chip seal design procedures to estimate aggregate application rates. Some of these parameters can also be used for quality measurement practices and comparative performance evaluations of chip seals.

The sieve analysis of the aggregates was performed in accordance with AASHTO T 27 and AASHTO T 11. The bulk specific gravities of the aggregates were determined in accordance with AASHTO T 84 and AASHTO T 85. The standard test method described in

AASHTO T 19 was used to determine the bulk density (unit weight) and voids in unit volume of the aggregates. The flakiness index test was conducted in accordance with the procedure adopted by the Minnesota DOT for chip seal aggregates. This test is conducted on aggregates retained on sieves larger than the No. 4 sieve. The sieve sizes of 3/8 in, ¼ in, and No. 4 were used in this study, as the nominal maximum aggregate size used was 3/8 in. In this test, representative samples of aggregates retained on each respective sieve are tested through a metal plate with slotted openings. The 3/8 in, ¼ in, and No. 4 sieves have slot openings of 0.263 by 1.57 (width by length) in, 0.184 by 1.18 in, and 0.131 by 0.79 in, respectively. The flakiness index is calculated as the percent ratio of the total mass of particles passing through each slot opening to the total mass of tested aggregates (sum of passing and retained aggregates). AASHTO M 340 specifies three traffic classes based on AADT for emulsions used in chip seal applications. These traffic classes are defined as low-volume traffic for AADT less than 500; medium-volume traffic for AADT between 501 and 2,500; and high-volume traffic for AADT greater than 2,500. The maximum flakiness index limits for low-, medium-, and high-volume traffic levels are 35%, 30%, and 25%, respectively. The abrasion resistance of the aggregates was determined in accordance with AASHTO T 96. The maximum percent abrasion loss limits for low-, medium-, and high-volume traffic levels are 40%, 35%, and 30%, respectively, as specified in AASHTO M 340.

Chip Seal Design

The emulsion and aggregate application rates for the field projects were determined in accordance with AASHTO R 102. The board test described in the standard was used to find the aggregate quantity that forms a one-stone-thick layer for each project. The aggregate application rate from the board test was increased by 10% to aid in reducing the potential for aggregate pick-up by pneumatic rollers during the rolling operation. The emulsion application rate for each project was calculated using the following information: the percent embedment of the aggregates relative to the quantity and average depth of the aggregate application rate from the board test; the specific gravity and unit weight of the aggregates; and the percent of the emulsion residue. The calculation also included a correction factor based on the traffic level. As indicated earlier, AASHTO R 102 uses AADT to classify traffic levels, but VDOT classifies routes based on the average daily traffic (ADT). For this study, the traffic for the project sites was assumed to be uniform throughout a year; thus, ADT was assumed to be equal to AADT. With this assumption, all routes in this study could be classified as low-traffic volume routes except for the routes for Projects 2 and 8 that can be classified as medium-traffic volume routes. Moreover, all projects were assumed to have a slightly porous and oxidized existing surface condition, which required no adjustments to the emulsion application rates.

Field Data Collection

The short-term performance of the field projects was monitored for up to 1.2 years, starting shortly after construction. Macrotexture surveys were performed 4 times (3 times in some projects) during the course of the study. A Sideway-Force Coefficient Routine Investigation Machine (SCRIM) was used to collect the macrotexture data. The macrotexture, expressed in terms of mean profile depth, was generated from the SCRIM data collected from the

left wheel path for every 0.1 m. The macrotexture was measured using a single-spot laser system from a single pass of the SCRIM over the entire length of a given project.

RESULTS AND DISCUSSION

Emulsion Properties

Emulsion Viscosity

Figures 1 and 2 show the viscosity measurements of the emulsions for sprayability and drain-out resistance characteristics, respectively. The results for Project 1 were not available due to testing issues. As shown, the emulsions met the limits specified in NCHRP Project 09-50 (Kim et al., 2017) for both properties. The results mean that the emulsions should have uniform sprayability during construction and resist flowing off the pavement surface once placed in the field. No challenges or issues regarding these two properties were reported or observed from the field projects.

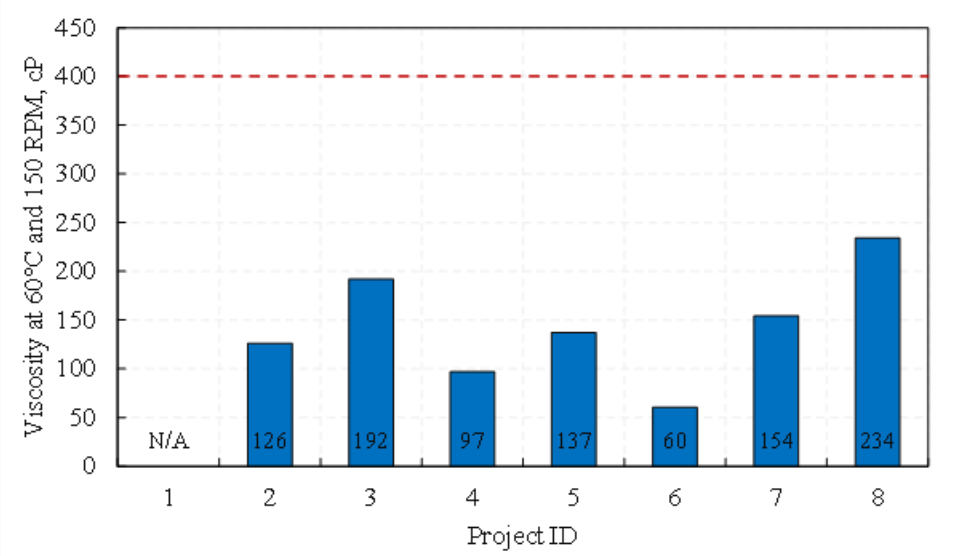

Figure 1. Viscosity of the Emulsions for Sprayability. The red dashed line indicates the maximum limit in accordance with NCHRP Project 09-50 (Kim et al., 2017). RPM = revolutions per minute; N/A = not available.

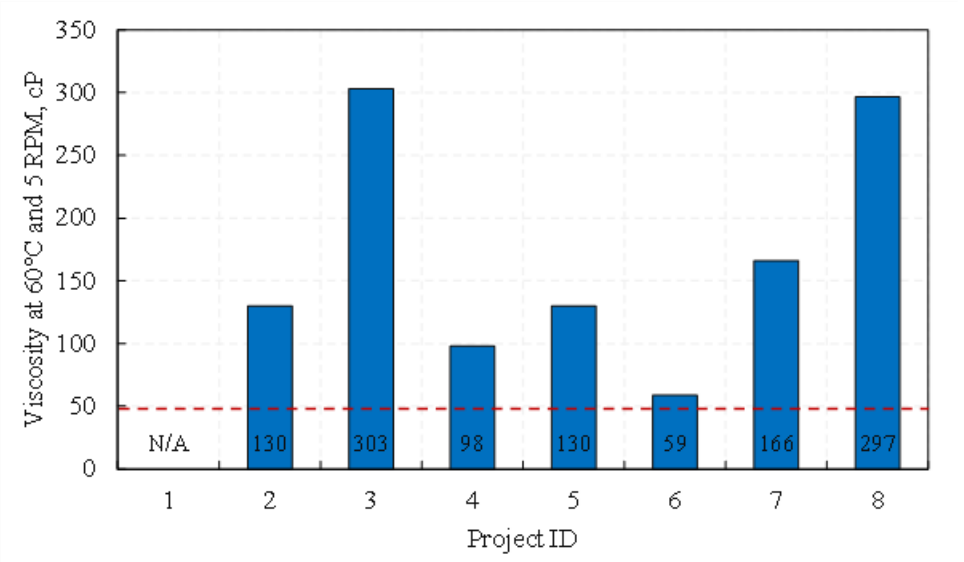

Figure 2. Viscosity of the Emulsions for Drain-Out Resistance. The red dashed line indicates the minimum limit in accordance with NCHRP Project 09-50 (Kim et al., 2017). RPM = revolutions per minute; N/A = not available.

Emulsion Residue Content

Figure 3 shows the residual asphalt contents of the emulsions. The overall average residual content was 67.9% by the weight of the emulsion, with a range of 67.1% to 69.1%. All emulsions met VDOT's specification requirement of at least 65% residue content for emulsions used in chip seal applications. The tests were repeatable, with an average coefficient of variation of 1%.

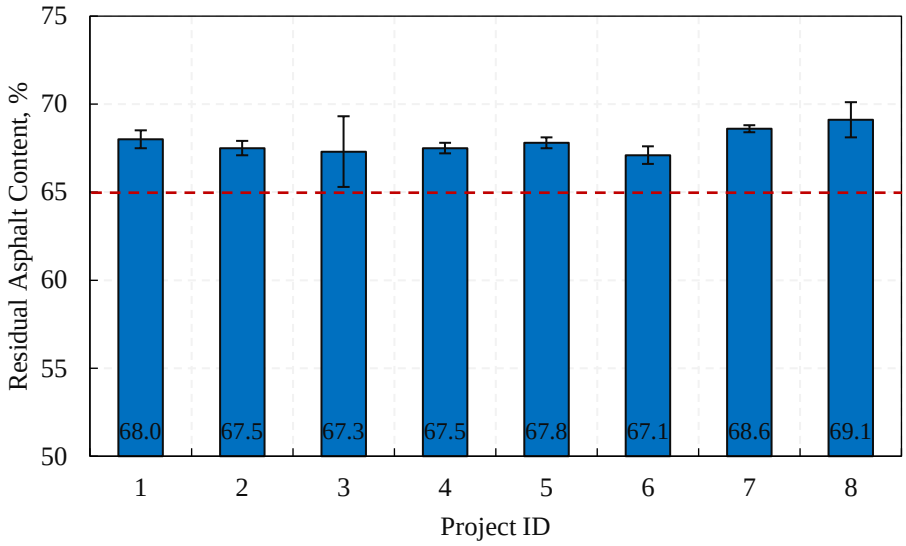

Figure 3. Residual Asphalt Contents of the Emulsions. I-bars indicate ±1 standard deviation. The red dashed line indicates VDOT's specification limit.

Emulsion Residue Rheology

Figure 4 shows the high- and low-temperature continuous PG of the emulsions (residue) determined in accordance with AASHTO MP 37. With regard to the PG of 67-25 as an adequate PG for emulsions used in chip seal applications in Virginia, only three of the eight emulsions met the high-temperature PG requirement of 67°C. On the other hand, only three of the eight failed to meet the low-temperature PG requirement of -25°C. The figure also shows that only two emulsions (from Projects 2 and 5) met the requirements of both temperatures as specified in AASHTO MP 37.

Figure 5 shows the J_{nr} values of the emulsions (residue) at a stress level of 3.2 kPa and a temperature of 67°C. As shown, all emulsions exceeded the maximum J_{nr} value of 8 kPa^{-1} established for low-volume traffic roads by Kim et al. (2017) in NCHRP Project 09-50. This observation indicates that the emulsions may contribute to a high bleeding potential of chip seals in the field.

Figure 6 shows the |G*| values of the emulsions (residue) at the δc of 45°. As shown, five of the eight emulsions were adequate for high-volume traffic roads, and the remaining three were adequate for medium-volume traffic roads from the aggregate loss susceptibility perspective, as specified by Kim et al., 1917) in NCHRP Project 09-50. As indicated earlier, the routes chip sealed in this study can be classified as low-traffic volume routes, except for Project 2 and 8 routes that can be classified as medium-volume traffic routes in accordance with the NCHRP Project 09-50 (Kim et al., 2017) and AASHTO R 102 classifications. This indicates that from the aggregate loss susceptibility perspective, the emulsions were of a high quality relative to the routes on which they were used.

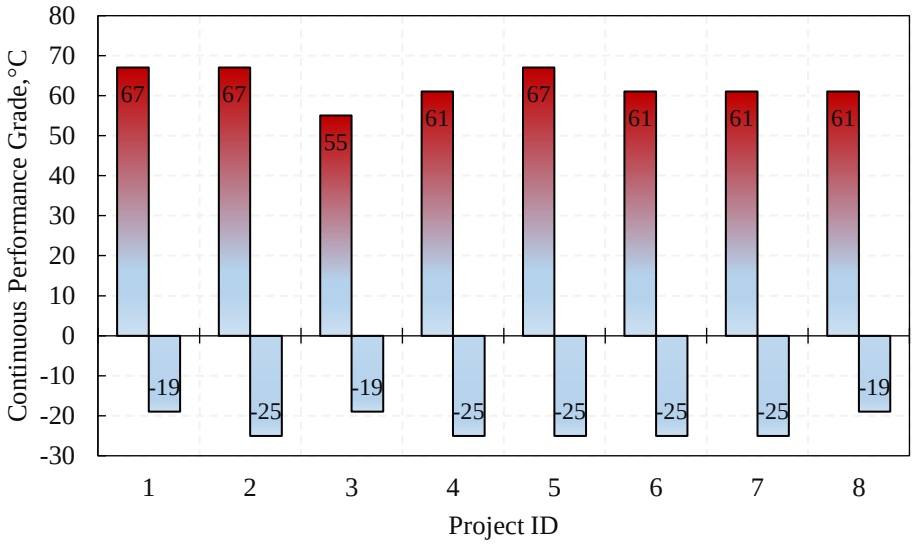

Figure 4. Continuous Performance Grades of the Emulsions (Residue) at High and Low Temperatures

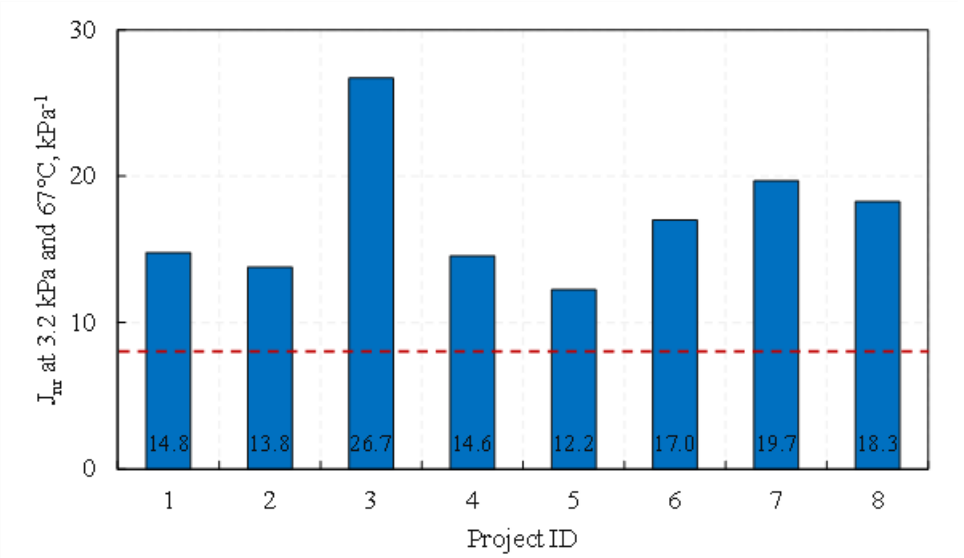

Figure 5. Non-Recoverable Creep Compliance (J_{nr}) Values of the Emulsions (Residue). The red dashed line indicates the maximum J_{nr} value limit for low-traffic volume roads in accordance with NCHRP Project 09-50 (Kim et al., 2017).

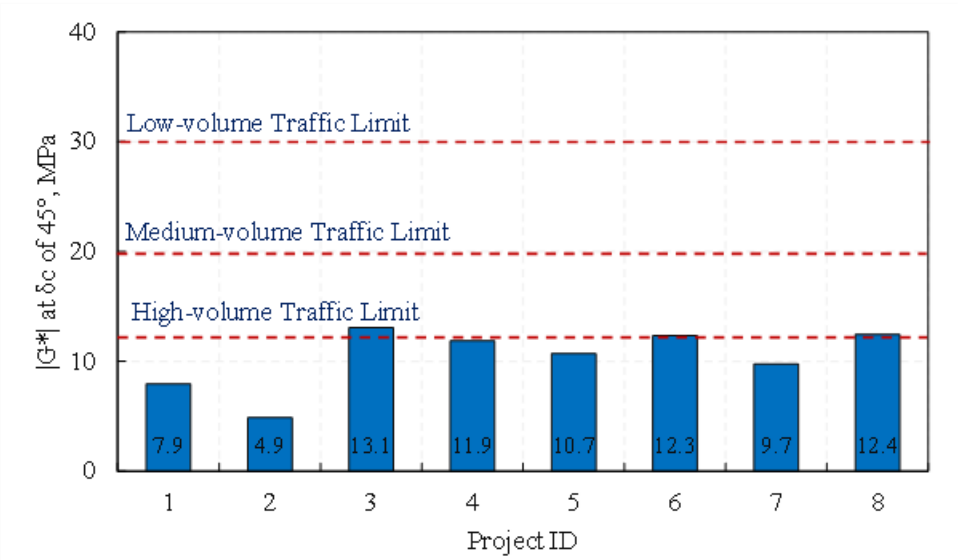

Figure 6. Dynamic Shear Modulus |G*| Values of the Emulsions at the Critical Phase Angle (δc) of 45°C. Dashed lines show the maximum |G*| traffic limits in accordance with NCHRP Project 09-50 (Kim et al., 2017).

Aggregate Properties

Table 2 shows the gradations for the first (coarse) layer aggregate application of the chip seals and the VDOT boundary sieve size requirements for Grade 8P aggregates. From the table, the aggregates from five projects did not meet VDOT's specification. Of particular concern are the gradations with high amounts of fines (for Projects 3, 6, and 7), as quantified by the percent passing the No. 200 sieve. The fines have a detrimental effect on the performance of chip seals by weakening the adhesive bonds between aggregates and emulsions.

Table 2. Gradations for the First (Coarse) Layer Aggregate Application

Sieve	Project ID								VDOT Specification
	1	2	3	4	5	6	7	8	
1/2 in	99.8	99.2	99.5	100.0	99.3	100.0	100.0	100.0	100
3/8 in	93.1	89.4	88.0	86.8	89.6	96.8	93.0	87.7	75-100
1/4 in	57.9	51.2	38.1	42.5	45.6	55.6	50.3	42.3	--
No. 4	32.8	27.8	16.6	16.7	19.7	28.0	26.6	19.0	5-30
No. 8	6.9	5.4	6.7	1.9	2.5	6.6	11.9	3.0	Max. 5
No. 16	4.1	3.2	4.8	1.4	1.8	4.0	7.8	2.1	--
No. 30	3.0	2.5	4.1	1.2	1.6	3.5	5.6	1.8	--
No. 50	2.4	2.1	3.8	1.0	1.5	3.2	4.4	1.6	--
No. 100	1.7	1.5	3.3	0.8	1.4	3.0	3.7	1.4	--
No. 200	1.0	0.9	2.4	0.6	1.2	2.8	3.1	1.2	Max. 1.5

Red text indicates values that did not meet the VDOT specification. -- = not specified.

Table 3 shows the gradations for the second (fine) layer aggregate application of the chip seals and the VDOT boundary sieve size requirements for Grade B and No. 9 aggregates. As indicated earlier, Project 3 was a single-layer chip seal application and thus did not include the fine aggregate application. The table shows that only one source (Project 7) did not meet the specification limits with respect to the percent passing the No. 4 sieve.

VDOT gradation requirements for chip seal aggregates were compared to the gradation requirements for chip seal aggregates specified in AASHTO M 340, as shown in Table 4. VDOT gradation requirements for Grade 8P aggregates (for the first layer application) are similar to the Type B gradation requirements in AASHTO M 340. However, Type B gradation has stricter requirements for the 3/8 in, No. 30, and No. 200 sieves. Chip seal aggregates with more uniform gradations and less fines are desirable for better performance in the field. In addition, VDOT has one type of gradation specified for chip seal applications, whereas AASHTO M 340 has four gradation types. Such flexibility of having different gradation types can provide more benefits (cost and performance) to VDOT compared to those of having only a single gradation. However, evaluation of that aspect was beyond the scope of this study.

Table 3. Gradations for the Second (Fine) Layer Aggregate Application

Sieve	Project ID								VDOT Specification
	1 (No. 9)	2 (No. 9)	3	4 (B)	5 (B)	6 (No. 9)	7 (No. 9)	8 (No. 9)	
1/2 in	100.0	100.0	-	100.0	100.0	100.0	100.0	100.0	--
3/8 in	100.0	100.0	-	100.0	100.0	100.0	100.0	100.0	Min.100 (B and No. 9)
1/4 in	99.8	99.8	-	99.9	99.5	99.5	93.8	100.0	--
No. 4	89.5	89.2	-	99.6	98.6	93.6	73.2	92.6	94-100 (B) or 85-100 (No. 9)
No. 8	12.7	14.2	-	91.2	69.0	26.0	21.0	16.0	10-40 (No. 9)
No. 16	3.9	2.8	-	78.0	45.1	6.4	6.4	5.1	Max. 16 (No. 9)
No. 30	2.6	1.4	-	52.3	28.2	3.8	3.1	3.2	--
No. 50	2.0	0.9	-	21.2	16.2	3.3	2.1	2.5	Max. 5 (No. 9)
No. 100	1.6	0.7	-	8.1	7.5	3.0	1.7	2.0	Max. 10 (B)
No. 200	1.1	0.6	-	1.9	3.9	2.8	1.5	1.6	Max. 5 (B and No. 9)

Red text indicates value that did not meet the VDOT specification. - = indicates no application of the fine layer aggregate; -- = not specified.

Table 4. AASHTO M 340 Gradation Requirements for Chip Seal Aggregates

Sieve	A	B	C	D[a]
3/4 in	100			
1/2 in	90-100	100		
3/8 in	5-30	90-100	100	100
No. 4	0-10	5-30	90-100	0-65
No. 8		0-10	5-30	0-15
No. 16	0-2		0-10	0-10
No. 30		0-2		
No. 50			0-2	0-6
No. 200	0-1	0-1	0-1	0-3

[a] Limit use to traffic levels less than 500 AADT. AADT = annual average daily traffic.

VDOT gradations for Grade B and No. 9 aggregates used for the second (fine) layer application are finer than the gradations specified in AASHTO M 340. Grade B and No. 9 aggregates in VDOT chip seal applications are mainly intended to be used as "tools" to provide an additional locking aid to the first layer aggregates, promoting an extended chip seal service life. They can also be used to avoid emulsion pick-up by tires and as a corrective measure in case of deficiencies observed with the first layer application.

Table 5 shows the properties of the first layer aggregates measured as part of this study. The first three properties in Table 5 are used as input parameters to determine the application rate for an emulsion in accordance with AASHTO R 102. The last two properties in Table 5 are the properties specified in AASHTO M 340 for durable chip seal performance. As indicated earlier, in accordance with AASHTO M 340, the maximum flakiness index limits for low-, medium-, and high-volume traffic levels are 35%, 30%, and 25%, respectively. From Table 5, all aggregates are suitable for high-volume traffic levels except for the aggregates used in Projects 1 and 7, which are suitable for medium-volume traffic levels. This indicates that from the perspective of the flakiness ratio, the aggregates were of a high quality relative to the routes on which they were applied. Likewise, AASHTO M 340 specifies the maximum percent abrasion loss limits for low-, medium-, and high-volume traffic levels as 40%, 35%, and 30%, respectively. From Table 5, all aggregates are suitable for high-volume traffic levels except for the aggregates used in Projects 1 and 2, which are suitable for medium-volume traffic levels. This indicates that from the perspective of the resistance to abrasion loss, the first layer aggregates were of a high quality relative to the routes on which they were used.

Table 6 shows the properties of the second (fine) layer aggregates measured as part of this study. Similar to the comparison analysis conducted for the first layer aggregates, the results indicate that from the perspective of the flakiness ratio and resistance to abrasion loss, the second layer aggregates were also of a high quality relative to the routes on which they were used.

Table 5. Properties of the First Layer Aggregates

	Project ID							
Aggregate Property	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Bulk Specific Gravity	2.581	2.592	2.699	2.712	2.708	2.701	2.717	2.987
Voids in Loose Aggregate, %	43.9	55.8	42.4	43.4	42.7	42.4	42.8	43.8
Loose Unit Weight, kg/m^3	1446.1	1215.9	1551.9	1532.4	1549.5	1551.9	1550.4	1674.6
Flakiness Ratio, %	25.9	19.4	18.9	20.9	24.8	18.5	29.5	23.6
Abrasion Loss, %	33.3	32.5	27.7	17.3	17.8	15.7	15.2	19.1

Table 6. Properties of the Second (Fine) Layer Aggregates

Aggregate Property	Project ID							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Bulk Specific Gravity	2.757	2.583	-	2.647	2.601	2.648	2.464	2.908
Voids in Loose Aggregate, %	45.9	48.3	-	N/A	43.2	41.7	23.3	45.1
Loose Unit Weight, kg/m^3	1488.6	1333.3	-	N/A	1475.1	1542	1886.6	1595
Flakiness Ratio, %	25.2	21.1	-	N/A	20.4	22.3	37.6	25.6
Abrasion Loss, %	32.5	23	-	N/A	31.5	18.2	20.4	26.4

- = indicates no application of the fine layer aggregate; N/A = not available.

Chip Seal Design

The chip seal projects in this study consisted of VDOT's modified single-layer applications except for Project 3, which was a single-layer chip seal application. Although the chip seal design procedure in AASHTO R 102 is mainly used for single-layer chip seal applications, it can still be used for modified single-layer chip seals, with each layer being treated as a single-layer chip seal application. As indicated, the main intent for the second layer application is to provide an additional locking aid to the aggregates from the first layer application so that a more durable chip seal application is achieved. To achieve this, the first layer chip seal application should have the optimal microstructure (a one-stone-thick layer with a proper aggregate orientation and aggregate embedment). Any deficiencies resulting from improper application rates (e.g., higher aggregate application rates with higher emulsion application rates) in the first layer will lead to an unstable chip seal performance structure, thereby hindering achievement of the goal of the second layer application.

Figure 7 shows the emulsion application rates for the first layer application on the projects as determined in accordance with AASHTO R 102. VDOT's chip seal specification prescribes an emulsion application rate of 0.17 gal/sy for the first layer application of modified single-layer chip seals. The emulsion application rates for unmodified single-layer chip seals range from 0.20 to 0.35 gal/sy in accordance with the procedure referenced in VDOT's chip seal specification. With regard to the modified single-layer chip seal projects, VDOT's fixed emulsion application rate of 0.17 gal/sy is lower than the rates determined in accordance with AASHTO R 102 by an average rate of 0.11 gal/sy, with a range of 0.09 to 0.14 gal/sy. For Project 3, which is a single-layer chip seal project, the emulsion application rate (0.30 gal/sy) determined in accordance with AASHTO R 102 fell between the range (0.20 to 0.35 gal/sy) indicated in the procedure referenced in VDOT's chip seal specification.

Figure 8 shows the aggregate application rates for the first layer application of the projects as determined in accordance with AASHTO R 102. VDOT's chip seal specification prescribes an aggregate application rate of 15 lb/sy for the first layer application of modified single-layer chip seals. The aggregate application rates for unmodified single-layer chip seals ranged from 20 and 25 lb/sy in accordance with the procedure referenced in VDOT's chip seal specification. With regard to the modified single-layer chip seal projects, VDOT's fixed aggregate application rate of 15 lb/sy was lower than the rates determined in accordance with AASHTO R 102 by an average rate of 2.9 lb/sy, with a range of 0.8 to 4.5 lb/sy. For Project 3, which is a single-layer chip seal project, the aggregate application rate (18.7 lb/sy) determined in accordance with AASHTO R 102 was lower than the low end of the aggregate application range (20 to 25 lb/sy) indicated in the procedure referenced in VDOT's chip seal specification.

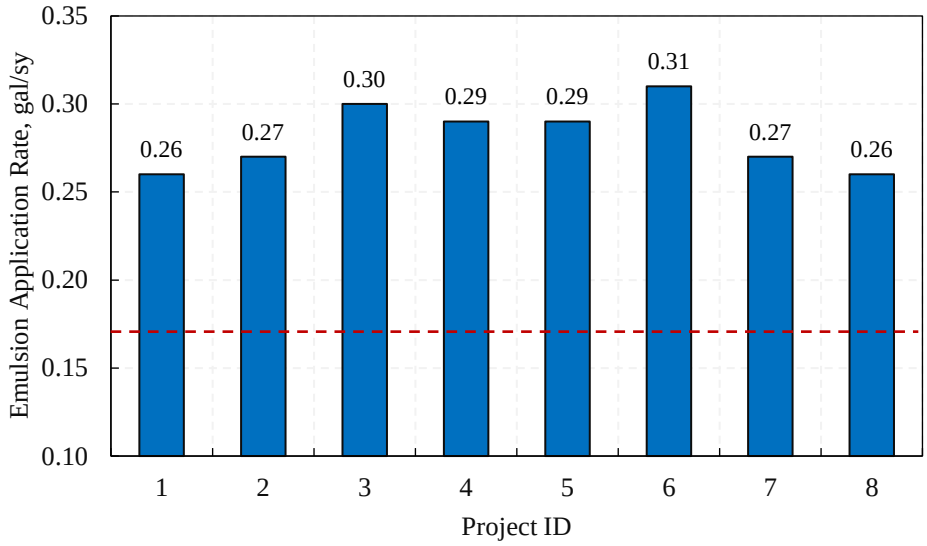

Figure 7. Emulsion Application Rates for the First Layer Application in Accordance With AASHTO R 102. The red dashed line indicates VDOT's fixed emulsion application rate of 0.17 gal/sy for the first layer application of modified single-layer chip seals. Project 3 was a single-layer chip seal with VDOT's design application rate ranging from 0.20 to 0.35 gal/sy.

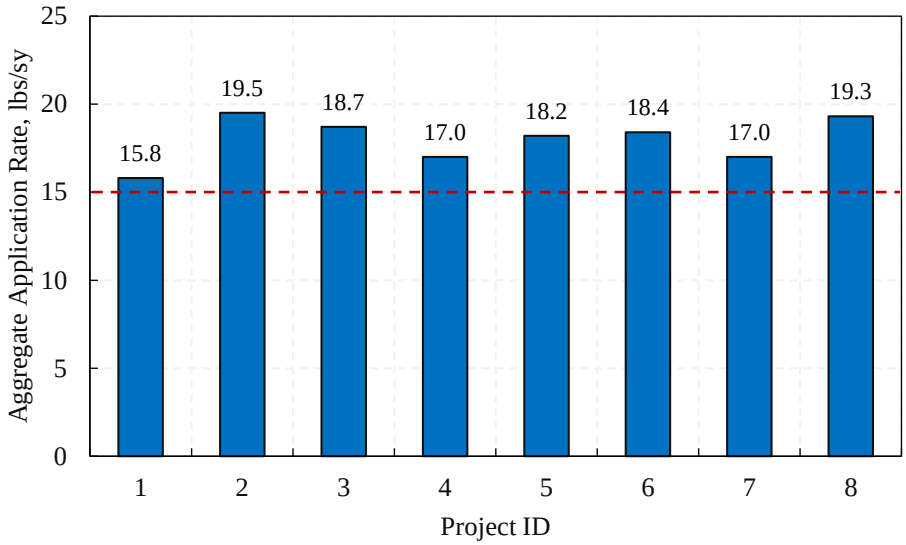

Figure 8. Aggregate Application Rates for the First Layer Application in Accordance with AASHTO R 102. The red dashed line indicates VDOT's fixed aggregate application rate of 15 lb/sy for the first layer application of modified single-layer chip seals. Project 3 was a single-layer chip seal, with VDOT's design application rate ranging from 20 to 25 lb/sy.

Figure 9 shows the emulsion application rates for the second layer application of the projects as determined in accordance with AASHTO R 102. VDOT's chip seal specification prescribes an emulsion application rate of 0.15 gal/sy for the second layer application of modified single-layer chip seals. VDOT's fixed emulsion application rate was comparable to the rates determined in accordance with AASHTO R 102. Except for Project 7, VDOT's fixed emulsion rate was lower by an average rate of 0.04 gal/sy, with a range of 0.02 to 0.06 gal/sy. For Project 7, VDOT's fixed emulsion rate was higher by 0.05 gal/sy.

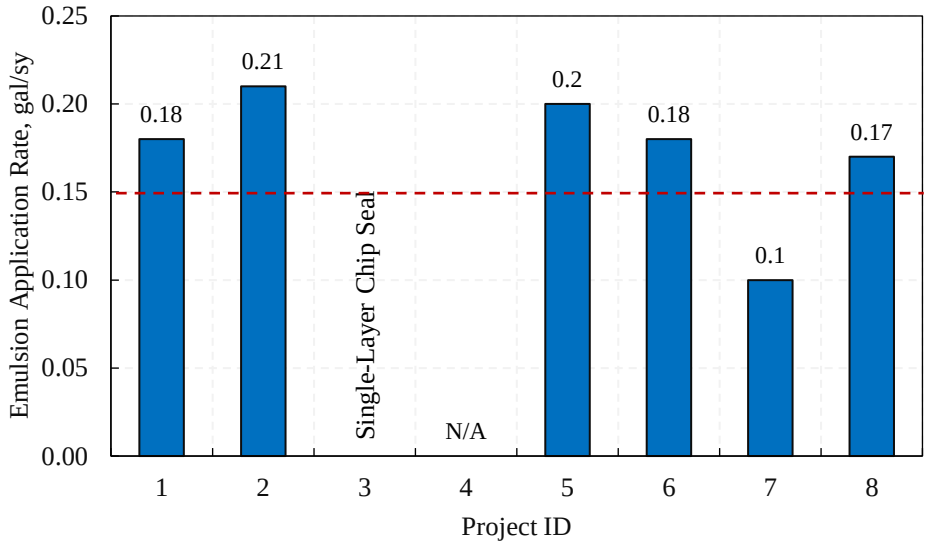

Figure 9. Emulsion Application Rates for the Second Layer Application in Accordance With AASHTO R 102. The red dashed line indicates VDOT's fixed emulsion application rate of 0.15 gal/sy for the second layer application of modified single-layer chip seals. Project 3 was a single-layer chip seal application. N/A = not available.

Figure 10 shows the aggregate application rates for the second layer application of the projects as determined in accordance with AASHTO R 102. VDOT's chip seal specification prescribes district-dependent aggregate application rates. For Projects 6 through 8, the prescribed aggregate application rate is 12 lb/sy for the second layer application of modified single-layer chip seals and is 10 lb/sy for the rest of the projects. From Figure 10, VDOT's fixed aggregate application rates were comparable to the rates determined in accordance with AASHTO R 102.

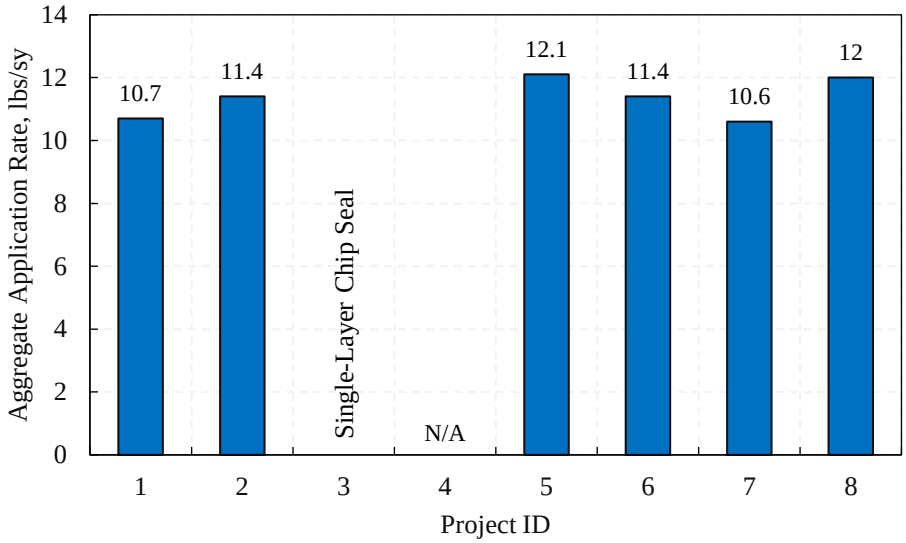

Figure 10. Aggregate Application Rates for the Second Layer Application in Accordance With AASHTO R 102. Project 3 was a single-layer chip seal application. For Projects 6-8, VDOT's prescribed application rate was 12 lb/sy and for the rest of the projects was 10 lb/sy. N/A = not available.

Table 7 shows the actual field application rates for the chip seal materials, calculated using the plate test results. The plate tests results were not available for the majority of the projects because either (1) the plate tests were conducted for another project within the same chip seal schedule, but not for the specific project included in this study, or (2) the plate tests were not conducted as the district(s) relied on the contract quantities. Nevertheless, it is evident from the table that the first layer emulsion application rates of the five projects were close to the VDOT prescribed application rate of 0.17 gal/sy but significantly lower than the rates calculated in accordance with AASHTO R 102. For the first layer aggregate application rates, the plate test results were significantly lower than the VDOT prescribed application rate of 15 lb/sy and the AASHTO R 102 measured rates except for Project 4, which was comparable to the rates indicated by both standards.

The second layer application rates of the modified single-layer chip seals were available for only two projects (Projects 4 and 7). The second layer emulsion application rates for both projects were comparable to VDOT's prescribed application rate of 0.15 gal/sy. The second layer aggregate application rates of 5.5 lb/sy and 9.0 lb/sy for Project 4 and Project 7, respectively, were lower than VDOT's prescribed application rates of 10 lb/sy and 12 lb/sy, respectively. The rates based on AASHTO R 102 were not available for Project 4. For Project 7, the emulsion application rate of 0.1 gal/sy from AASHTO R 102 was lower than the field emulsion application rate of 0.15 gal/sy. The field aggregate application rate of 9 lb/sy for Project 7 was deemed comparable to the aggregate application rate of 10.6 lb/sy determined from AASHTO R 102.

Table 7. Field Application Rates for the Chip Seal Materials

	First Layer		Second Layer	
Project ID	**Emulsion, gal/sy**	**Aggregate, lb/sy**	**Emulsion, gal/sy**	**Aggregate, lb/sy**
1	0.16	10.6	N/A	N/A
2	0.14	9.2	N/A	N/A
3	N/A	N/A	-	-
4	0.16	16.6	0.17	5.5
5	0.17	12.1	N/A	N/A
6	N/A	N/A	N/A	N/A
7	0.15	12.1	0.15	9.0
8	N/A	N/A	N/A	N/A

- = no application of the fine layer aggregate; N/A = not available.

Field Performance

Macrotexture has been used as a metric for evaluating the performance of chip seals with regard to the common modes of distress and the quality of construction (Adams and Kim, 2014; Aktas et al., 2011; Chaturabong et al., 2015; Gurer et al., 2012; Roque et al., 1991; Seitllari and Kutay, 2018; Shuler et al., 2011; Transit New Zealand, 2005). For instance, a macrotexture depth of 0.9 mm at the end of a 1-year service life in the field is considered a performance criterion limit for re-treating New Zealand's chip seal projects (Transit New Zealand, 2005), which was shown to be applicable to evaluate chip seal performance in the United States (Gransberg, 2007). The percent loss in macrotexture is also correlated with aggregate loss and bleeding distresses (Adams and Kim, 2014; Chaturabong et al., 2015). Moreover, macrotexture

and average least dimension of aggregates are used to calculate the percent embedment depth of aggregates in chip seals, particularly for single-layer chip seals (Shuler et al., 2011).

Figure 11 shows the progression of macrotexture with traffic at a network level. For a given project, the traffic (vehicle) count corresponding to each macrotexture measurement was calculated by multiplying ADT with the time of measurement (the length of time in days the treatments had been in place). The figure shows that the macrotexture levels off around a depth of approximately 1 mm, despite an increase in traffic counts. This suggests that the macrotexture depth of 1 mm can be used as a performance criterion to evaluate the chip seal performance. However, the macrotexture depth of 0.9 mm is deemed more appropriate than the macrotexture depth of 1 mm to evaluate the performance of chip seals in this study. This selection was made to incorporate a safety factor and to account for the variability in the measurements to some extent. It is also worth noting that the macrotexture depth of 1 mm is reasonably close to New Zealand's 0.9 mm performance criterion.

Figure 12 shows the progression of macrotexture for each project with up to a 1.2-year service life in the field. As expected, the magnitude of macrotexture decreased over time (or with trafficking). For some projects, such as Projects 1 and 3, there was a sudden drop in the magnitude of macrotexture, which suggests that the microstructure (aggregate orientation and embedment) was unstable for these chip seals, indicating potential aggregate loss and bleeding problems. With regard to the macrotexture depth of 0.9 mm, one-half of the projects (1, 3, 6, and 7) have fallen below the 0.9-mm threshold in the year after construction. It is noted that the 0.9-mm threshold is determined based on the trend seen in the collected data and used as a guide to indicate performance. Further studies are needed to investigate the viability of this threshold.

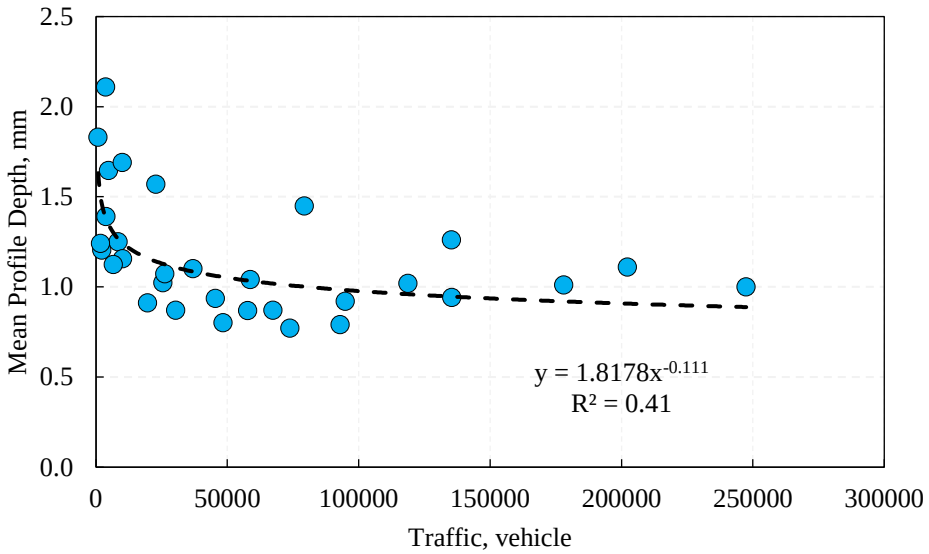

Figure 11. Macrotexture Progression With Traffic

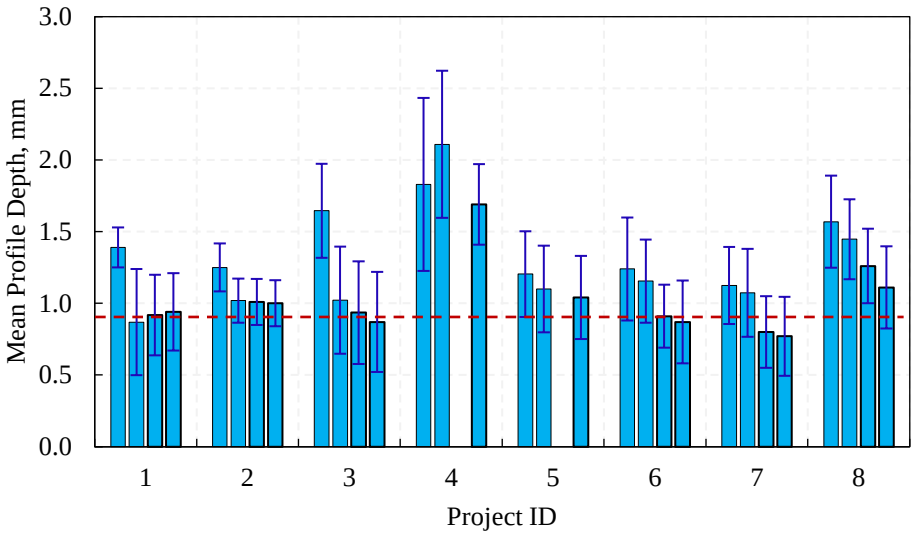

Figure 12. Macrotexture Progression for Chip Seal Projects for Up to a 1.2-Year Service Life. The first of the four bars for each project corresponds to a measurement taken within 1 month after construction. The other three bars correspond to the measurements taken at approximately a 0.5-, 0.8-, and 1.2-year service life in the field. The red dashed line indicates a macrotexture performance criterion determined based on the data trends observed in this study. The third measurements for Projects 4 and 5 were not available.

CONCLUSIONS

- *The rheology-based emulsion residue evaluations in this study indicated that the emulsions used in chip seals may not be suitable for the conditions (traffic and climate) in which they were used.* Six of the eight emulsions did not meet the performance-grading criteria specified in AASHTO MP 37.

- *The physical characteristics of the aggregates used in the chip seals were suitable for the conditions (traffic) in which they were used.* All aggregate sources evaluated in this study met or exceeded the performance criteria specified in AASHTO M 340. However, VDOT's specification does not specify traffic-based limits for the characteristics of chip seal aggregates.

- *VDOT's referenced chip seal design methodology for single-layer chip seals and VDOT's prescribed emulsion and aggregate application rates for modified single-layer chip seals may not be appropriate.* The design aggregate and emulsion application rates determined in accordance with AASHTO R 102 were considerably higher for the first layer of the modified single-layer chip seals evaluated in this study. The design application rates from AASHTO R 102 are deemed to be a better starting point for chip seal applications than those of indicated approximate design application rates in VDOT's specification.

- *More vigorous quality control measurement practices are vital for improved or optimal performance.* The field aggregate and emulsion application rates were not determined for the single-layer chip seal project and two of the seven modified chip seal projects evaluated in this study. In addition, the field aggregate and emulsion application rates were not

determined for the second layer applications of five of the seven modified chip seal projects evaluated in this study. Moreover, for the projects for which application rates were determined, the aggregate application rates were lower than those prescribed by VDOT.

RECOMMENDATIONS

1. *VDOT's Materials Divisions should consider adopting AASHTO MP 37 as the standard used for performance grading of emulsions (residues) for surface treatments.*

2. *VDOT's Materials Divisions should consider adopting traffic-based requirements for abrasion loss and the flakiness index as specified in AASHTO M 340.* The other referenced standards in AASHTO M 340 are already included in VDOT's specification.

3. *VDOT's Materials Divisions and the Virginia Transportation Research Council (VTRC) should plan and execute chip seal field trials designed in accordance with AASHTO R 102.* This will help assess further the viability of adopting AASHTO R 102 as the standard used for chip seal design.

4. *VDOT's Materials Division should explore the quality measurement practices that would lead to improving the service life of chip seals.*

IMPLEMENTATION AND BENEFITS

The researcher and the technical review panel (listed in the Acknowledgments) for the project collaborate to craft a plan to implement the study recommendations and to determine the benefits of doing so. This is to ensure that the implementation plan is developed and approved with the participation and support of those involved with VDOT operations. The implementation plan and the accompanying benefits are provided here.

Implementation

With regard to Recommendation 1, VDOT's Materials Division will deliberate internally on the necessity of adopting AASHTO MP 37 as the standard used for performance grading of emulsions for surface treatments considering the budget and resources needed. A decision is anticipated by December 2025.

With regard to Recommendations 2 and 3, VDOT's Materials Division with the help of VTRC will plan for field trials during the 2025 construction season to collect additional data for further evaluation of the recommendations.

With regard to Recommendation 4, VTRC will submit a research needs statement to Subcommittee A, Pavement Preservation and Management, of VTRC's Pavement Research Advisory Committee by fall 2024.

Benefits

Pavement preservation treatments, including chip seals, extend the service life of pavements through delaying deterioration by minimizing moisture infiltration and slowing down aging of the flexible pavements. This study identified potential areas of improvements for VDOT's chip seal practices and provided a set of recommendations for improving the quality of chip seal practices that could result in achieving the benefits associated with the treatment.

Recommendations 1 through 4 are geared toward ensuring the proper use of constituent materials, a robust design methodology, and quality control/assurance practices. Implementing these recommendations is anticipated to help achieve the desired outcome of chip seals: longer service life, larger cost savings, reduced user delays, and safer roads.

ACKNOWLEDGMENTS

The author is grateful to the following individuals who served on the technical review panel for this study: Mourad Bouhajja (Project Champion and Statewide Asphalt Program Manager, VDOT Materials Division); Kevin Chisnell (Pavement Manager, VDOT Lynchburg District); Tanveer Chowdhury (Maintenance Engineer, VDOT Richmond District); Jhony Habbouche (Senior Research Scientist, VTRC); Lewis Lloyd (Research Scientist, VTRC); and Bryan Smith (Asphalt Pavement Field Engineer, VDOT Materials Division). The author thanks Troy Deeds, Derek Lister, and Jennifer Samuels, of VTRC, and Danny Martinez Rodriguez, formerly of VTRC, for their outstanding efforts in sample collection and testing. The author also thanks Gerardo Flintsch and Edgar de Leon Izeppi of Virginia Tech Transportation Institute for their efforts in collecting and processing macrotexture data. Appreciation is also extended to Linda Evans of VTRC for her editorial support.

REFERENCES

Adams, J., and Kim, Y.R. Mean Profile Depth Analysis of Field and Laboratory Traffic-Loaded Chip Seal Surface Treatments. *International Journal of Pavement Engineering*, Vol. 15, No. 7, 2014, pp. 645-656.

Adams, J., and Kim, Y.R. *Development of a New Chip Seal Mix Design Method*. HWY-2008-04. North Carolina Department of Transportation, Raleigh, 2011.

Aktas, B., Gransberg, D., Riemer, C., and Pittenger, D. Comparative Analysis of Macrotexture Measurement Tests for Pavement Preservation Treatments. *Transportation Research Record: Journal of the Transportation Research Board*, No. 2209, 2011, pp. 34-40.

Boz, I., Kumbargeri, Y., and Kutay, M.E. Performance-Based Percent Embedment Limits for Chip Seals. *Transportation Research Record: Journal of Transportation Research Board*, No. 2673(1), 2019, pp. 182-192.

Boz, I., Kumbargeri, Y., Kutay, M.E., and Haider, S.W. *Establishing Percent Embedment Limits to Improve Chip Seal Performance*. No. SPR-1679. Michigan Department of Transportation, Lansing, 2018.

Buss, A.F., Guriguis, M., Claypool, B., Gransberg, D., and Williams, R.C. *Chip Seal Design and Specifications*. FHWA-OR-RD-17-03. Oregon Department of Transportation, Salem, 2016.

Chaturabong, P., Hanz, A.J., and Bahia, H. Development of Loaded Wheel Test for Evaluating Bleeding in Chip Seals. *Transportation Research Record: Journal of the Transportation Research Board*, No. 2481, 2015, pp. 48-55.

Cross, S.A., and Jakatimath, Y. *Evaluation of Cold In-Place Recycling for Rehabilitation of Transverse Cracking on US 412*. FHWA/OK 07 (04). Oklahoma Department of Transportation, Oklahoma City, 2007.

Das, B., and Sobham, K. *Principles of Geotechnical Engineering*. Cengage Learning, Boston, MA, 2013.

Gransberg, D. Using a New Zealand Performance Specification to Evaluate US Chip Seal Performance. *Journal of Transportation Engineering*, 133, No. 12, 2007, pp. 688-695.

Gransberg, D.D., and James, D.M. *NCHRP Synthesis of Highway Practice 342: Chip Seal Best Practices.* Transportation Research Board, Washington, DC, 2005.

Gurer, C., Karasahin, M., Cetin, S., and Aktas, B. Effects of Construction-Related Factors on Chip Seal Performance. *Construction and Building Materials*, Vol. 35, 2012, pp. 605-613.

Islam, S., and Hossain, M. Chip Seal With Lightweight Aggregates for Low-Volume Roads. *Transportation Research Record: Journal of the Transportation Research Board*, No. 2205, 2011, pp. 58-66.

Janisch, D.W., and Gaillard, F.S. *Minnesota Seal Coat Handbook.* MN/RC-1999-07. Minnesota Department of Transportation, Maplewood, 1998.

Johannes, P.T., and Bahia, H. Asphalt Emulsion Sprayability and Drain-Out Characteristics in Chip Seals: Evaluation With Viscosity at Variable Shear Rates. *Transportation Research Record: Journal of the Transportation Research Board*, No. 2361(1), 2013, pp. 80-87.

Johannes, P.T., Mahmoud, E., and Bahia, H. Sensitivity of ASTM D7000 Sweep Test to Emulsion Application Rate and Aggregate Gradation. *Transportation Research Record: Journal of the Transportation Research Board*, No. 2235, 2011, pp. 95-102.

Kim, Y.R., Adams, J., Castorena, C., Ilias, M., Im, J.H., Bahia, H., Chaturabong, P., Hanz, A., and Johannes, P.T. *Performance-Related Specifications for Emulsified Asphaltic Binders*

Used in Preservation Surface Treatments. NCHRP Project 09-50. Transportation Research Board, Washington, DC, 2017.

Kumbargeri, Y.S., Kutay, M.E., and Boz, I. Effect of Percent Embedment on Chip Seal Performance Using FE Modeling. In *Advances in Materials and Pavement Performance Prediction,* pp. 583-586. CRC Press, 2018a.

Kumbargeri, Y.S., Boz, I., and Kutay, M.E. Performance Based Design Procedure for Chip Seal Projects. In *Advances in Materials and Pavement Prediction*, pp. 575-578. CRC Press, 2018b.

Kumbargeri, Y., Boz, I. and Kutay, M.E. Comparative Investigation of Hot-Applied and Emulsion-Based Chip Seal Treatments Using Image Processing Techniques and Performance tests. *Journal of Transportation Engineering, Part B: Pavements*, Vol. 147, No. 3, 2021, p. 04021039.

Kumbargeri, Y., Boz, I., and Kutay, M.E. Investigating the Effect of Binder and Aggregate Application Rates on Performance of Chip Seals via Digital Image Processing and Sweep Tests. *Construction and Building Materials*, Vol. 222, 2019, pp. 213-221.

Kumbargeri, Y., Boz, I., Kutay, M.E., and Heidelberg, A. A Study on the Effects of Aggregate Shape and Percent Embedment on Chip Seal Performance via Image-Based Finite Element Analysis. *International Journal of Pavement Engineering*, Vol. 21, No. 8, 2020, pp. 1002-1011.

Lee, J., and Kim, Y. Performance-Based Uniformity Coefficient of Chip Seal Aggregate. *Transportation Research Record: Journal of the Transportation Research Board*, No. 2108, 2009, pp. 53-60.

Marasteanu, M.O., and Anderson, D.A. Improved Model for Bitumen Rheological Characterization. In *Eurobitume Workshop on Performance Related Properties for Bituminous Binders*, Vol. 133. European Bitumen Association, Brussels, Belgium, 1999.

Maupin, G.W., and Payne, C.W. *Evaluation of Modified Single Seal Surface Treatments*. VTRC 95-R23. Virginia Transportation Research Council, Charlottesville, 1995.

McLeod, N. A General Method of Design for Seal Coats and Surface Treatments. *Proceedings of the Association of Asphalt Paving Technologists*, Vol. 38, 1969, pp. 537-630.

Miller, T., Arega, Z., and Bahia, H. Correlating Rheological and Bond Properties of Emulsions to Aggregate Retention of Chip Seals. *Transportation Research Record: Journal of the Transportation Research Board*, No. 2179, 2010, pp. 66-74.

Pierce, L.M., and Kebede, N. *Chip Seal Performance Measures: Best Practices*. WA-RD 841.1. Washington State Department of Transportation, Olympia, 2015.

Rizzutto, S.J., La Bar, J., Johannes, P.T., and Bahia, H. Use of a Variable Rate Spray Bar to Minimize Wheel Path Bleeding for Asphalt-Rubber Chip Seal Applications. *Journal of Materials in Civil Engineering*, Vol. 27, No. 3, 2015, p. 04014121.

Roque, R., Anderson, D., and Thompson, M. Effect of Material, Design, and Construction Variables on Seal-Coat Performance. *Transportation Research Record: Journal of the Transportation Research Board*, No. 1300, 1991, pp. 108-115.

Seitllari, A., and Kutay, M.E. Soft Computing Tools to Predict Progression of Percent Embedment of Aggregates in Chip Seals. *Transportation Research Record: Journal of the Transportation Research Board*, No. 2672(12), 2018, pp. 32-39.

Shuler, S., Lord, A., Epps-Martin, A., and Hoyt, D. *NCHRP Report 680: Manual for Emulsion-Based Chip Seals for Pavement Preservation*. Transportation Research Board, Washington, DC, 2011.

Texas Department of Transportation. *Seal Coat and Surface Treatment Manual*. Austin, 2010.

Transit New Zealand. *Chip Sealing in New Zealand*. Road Controlling Authorities, and Roading New Zealand, Wellington, 2005.

Wasiuddin, N.M., Marshall, A., Saltibus, N.E., Saber, A., Abadie, C., and Mohammad, L. Use of Sweep Test for Emulsion and Hot Asphalt Chip Seals: Laboratory and Field Evaluation. *Journal of Testing and Evaluation*, Vol. 41, No. 2, 2013, pp. 289-298.

Zaman, M., Gransberg, D., Bulut, R., Commuri, S. and Pittenger, D. *Develop Draft Chip Seal Cover Aggregate Specification Based on AIMS Angularity, Shape and Texture Test Results*. OTCREOS11.1-65-F. Oklahoma Department of Transportation, Oklahoma City, 2013.